IN THE CLAIMS:

1. (Original) A method of forming an interconnect on a semiconductor substrate, comprising:

forming a relatively narrow first structure in a dielectric formed on a semiconductor substrate;

forming a relatively wider second structure in said dielectric formed on the semiconductor substrate;

forming a liner in said first and second structures such that said first structure is substantially filled and said second structure is substantially unfilled; and

B1 forming a metallization over said liner to completely fill said second structure.

2. (Original) The method of claim 1, wherein said liner comprises one of a chemical vapor deposition (CVD) metal, a physical vapor deposition (PVD) metal and a plated liner.

3. (Original) The method of claim 1, wherein said liner comprises at least one of tungsten, aluminum, and titanium nitride.

4. (Original) The method of claim 1, wherein said metallization comprises copper.

5. (Original) A method of forming an interconnect on a semiconductor substrate, comprising:

forming a contact, including a slot, in a dielectric formed on a semiconductor substrate;

forming troughs into the dielectric, thereby to form a dual damascene structure;

depositing a conducting material on the dielectric;

depositing a metal over the conducting material to completely fill the slot and troughs;

removing the metal either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric; and

selectively removing the conducting material.

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6. (Previously Amended) The method of claim 5, wherein said dielectric comprises one of tetraethylorthosilicate (TEOS) oxide, silane oxide, and another low K polymer dielectric.

7. (Original) The method of claim 6, wherein said contacts comprise contacts formed between first and second metal levels formed on the semiconductor substrate.

8. (Original) The method of claim 5, wherein said conducting material comprises tungsten.

9. (Original) The method of claim 8, wherein the tungsten comprises chemical vapor-deposited (CVD) tungsten, a physical vapor deposition (PVD) tungsten, and a plated

tungsten.

10. (Currently Amended) The method of claim 5, wherein a thickness of the conducting material is adjusted so as to ~~completely~~ substantially fill the slot.

11. (Original) The method of claim 5, wherein said metal comprises copper.

12. (Original) The method of claim 5, wherein the metal is removed by chemical mechanical polishing (CMP).

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13. (Original) The method of claim 5, wherein said selectively removing comprises selectively removing said conductive material by a selective etch.

14. (Original) The method of claim 5, wherein said selectively removing comprises selectively removing said conductive material by a selective CMP.

15. (Previously Amended) The method of claim 5, further comprising:

repeating said depositing a conducting material; and

repeating said depositing a metal over the conducting material, thereby depositing subsequent said conducting material and said metal on the resulting structure.

16. (Original) A method of forming an interconnect on a semiconductor substrate, comprising:

forming troughs between first and second metal levels, including a slot, in a dielectric formed on a semiconductor substrate;

forming contacts in the dielectric, thereby to form a dual damascene structure;

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depositing a conducting material on the dielectric;

depositing a metal over the conducting material to completely fill the slot and the troughs;

removing the metal either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric; and

selectively removing the conducting material.

18. (Previously Added) The method of claim 16, wherein said conducting material comprises one of a chemical vapor deposition metal, a physical vapor deposition metal, and a plated liner.

19. (Previously Added) The method of claim 16, wherein said contacts comprise contacts formed between first and second metal levels formed on the semiconductor substrate.

20. (Previously Added) The method of claim 16, wherein said selectively removing comprises selectively removing said conductive material by a selective etch.

21. (Previously Added) The method of claim 1, wherein said relatively narrow first structure is not connected on said substrate to said relatively wider second structure.

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22. (Previously Added) The method of claim 1, wherein said forming a relatively wider second structure forms said wider structure on said substrate apart from said relatively narrow structure.

23. (Previously Added) The method of claim 5, wherein said contact is not connected in said substrate to said trough.

24. (Previously Added) The method of claim 5, wherein said forming troughs forms said troughs in said dielectric apart from said contact.